Design of Symmetrical Voltage Multiplier High Gain Interleaved DC to DC Converter for Photovoltaic Applications

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ABSTRACT

High voltage gain interleaved DC to DC boost converters are employed in Photovoltaic (PV) energy conversion for their structural advantage. The proposed converter builds upon the existing two-phase interleaved DC to DC boost converter, which is commonly used in utility grid integration circuits to minimize ripple current from the PV. The aim is to enhance the output voltage of the currently installed PV array in order to cater to high-power applications or grid integration. The key requirements include achieving high-efficiency power conversion and fully utilizing the potential of the PV system. The methods being proposed to increase the PV output voltage suffer from drawbacks such as low efficiency, complexity, and cost. In contrast, the suggested DC-DC converter boasts a remarkable efficiency of 96% and is capable of converting voltage from 25 V to 400 V for a power output of 400 W. The designed converter has been simulated in MATLAB software and the performance is compared to existing converters related to voltage stress, voltage gain against given duty cycle, and efficiency.

Keywords-high gain conversion; high-efficiency power conversion; interleaved DC to DC converter; photovoltaic system; high frequency switching

I. INTRODUCTION

Photovoltaic (PV) energy systems have gained increased attention in response to the global energy crisis. However, PV energy conversion systems suffer from poor conversion efficiency as a result of multiple conversion stages and high voltage difference between source and load. To address these challenges, a high voltage gain DC converter has been employed to enhance the poor voltage profile of PV. This section provides the requirements, topologies, control, and drawbacks of existing power converters for high voltage gain DC conversion. High voltage gain DC conversion is required for a variety of applications, including automobile power systems, uninterruptible power supply, multiport conversion, traction, and renewable integration [1]. The DC-DC converters needed for the first stage conversion in hybrid renewable integration into the utility grid are presented in [2], which specifies the need for high-gain DC-DC conversion in hybrid renewable integration. These converters also find usage in residential community applications for rooftop PV integration, DC charging of vehicles and DC power supplies [3]. Another important application for high gain non-isolated converters is interfacing renewables and energy storage with a DC microgrid. A wide range of topologies were developed in this

regard. Multiport converters are a promising attempt [4, 5], in which possible reduction in power electronic components is focused along with an efficient interface. Also, interleaving made the interface more reliable [6]. To achieve high gain, voltage multipliers are utilized [7, 8] in cascade with interleaved boost converters. Cascaded boost stages [8], quasi-Y-sources [9], switched inductors [10] have been developed for achieving high voltage gain with interleaved boost converters. The leakage inductance stresses switches in the flyback converter, which has easy construction and high voltage gain [11]. Energy-regeneration strategies have been applied to mitigate this stress. The phase-shifted full-bridge converter, on the other hand, generates higher input ripple currents and achieves a high voltage gain by using a higher turn ratio in the transformer [12, 13]. Electrolytic capacitors are employed in the phase-shifted full-bridge converter to reduce input current ripples.

Further opportunities in achieving higher efficiencies include soft switching and low duty cycle operation of the converter. Switching capacitor-based converter circuits [14, 15] like bridge type boost converters and clamped active dual boost operation converters provide zero voltage and zero current switching to obtain reduced switching losses. However, these converters have high transient current, significant switch conduction loss, and increased complexity [16] due to the additional switched capacitor cells. Modified switched-capacitor cells use soft-switching [17] to decrease switching loss and electromagnetic interference. Additionally, a coupled inductor approach with modified turn ratio was utilized in [18] to achieve a large step-up gain. Nevertheless, all currently used high voltage gain converters and ultra-boost converters still experience significant voltage stress [19] across the diode. Finally, efficient Maximum Power Point Tracking (MPPT) is needed to extract the maximum of the available renewable power. The converters developed in [20-22] use two-stage conversion with the first stage to extract maximum power and the second stage for desired voltage gain. Novel topologies include integrated conversion control for the required voltage gain and MPPT control [23-25]. Transformer included topologies based on low duty ratio were developed [26-28], which achieve high voltage gain at a duty ratio as low as 0.25. The existing topologies and control lack in either low duty operation or soft switched operation along with MPP extraction. Therefore, the need to develop an interface which achieves MPPT, high gain with a low duty cycle, and soft switching for higher efficiency is identified. The following are the novel contributions of this study towards integrating low voltage PV systems to high voltage DC bus:

- The developed converter achieves significant gain in voltage for lower duty cycles. This is possible because of the integration of a two-stage switching capacitor with a connected inductor, which effectively boosts the voltage gain.
- The converter achieves a reduction in conduction loss due to low duty operation.
- Minimized ripple in DC current due to interleaved connection of inductors.
- The converter achieves reduced switching losses due to facilitation of zero voltage switching by passive clamp circuit and zero current switching by intrinsic loss of the inductor.
- By regulating the current drop rate through leakage inductance, the converter mitigates issues related to the reverse recovery of the diode, ultimately leading to increased efficiency.

II. HIGH GAIN INTERLEAVED SYMMETRICAL BOOST DC DC CONVERTER

The proposed symmetrical multiplier based interleaved DC-DC converter for high voltage gain conversion with MPPT control is depicted in Figure 1. L_1, L_2 represent magnetizing inductances, D_1, D_2, D_3, D_4 represent multiplier cell diodes, C_1, C_2 represent multiplier cell capacitors. C_3, C_4 represent output side regulating capacitors, and S_1, S_2 represent power conversion switches. The conventional interleaved DC-DC converter is developed upon the proposed converter architecture by the addition of two additional capacitors and diodes. For this study, a 25 V and 250 Wp PV source with a load capable of dissipating 200 W power is considered. The duty cycle of the switch is a function of the MPPT voltage and current, which is measured continuously. Thus, maximum power is absorbed from the PV source at any given instant. The energy held in the inductor and capacitors, along with the energy in other switched capacitors, is transferred to output capacitors during the energy transfer period, allowing for achieving twice the voltage gain.

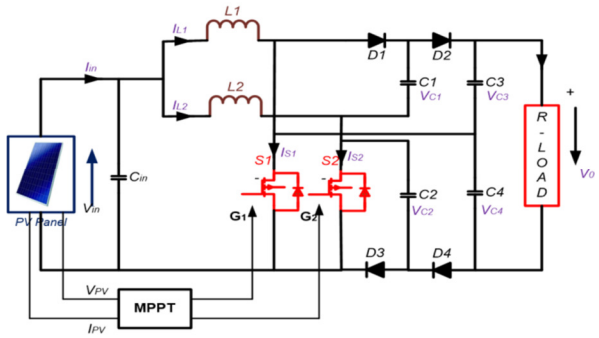


Fig. 1. Symmetrical voltage multiplier high gain interleaved DC-DC converter.

Compared to a traditional interleaved converter, the power switches and diodes experience less voltage stress. The integrated MPPT controller maximizes conversion rates while monitoring maximum power. When the duty cycle is greater than 0.5, a method of operation called "continuous conduction" is used. This is what makes the high voltage gain. For duty cycles less than half the cycle period, the circuit operates in an irregular conduction pattern. Therefore, a high voltage gain cannot be obtained. Also, the RMS current will be large in this case because the inductor, the blocking capacitor, and the capacitor do not share enough energy with each other.

1) Mode I: ($t_0 \leq t < t_1$)

The equivalent circuit during mode I involves switches S_1 and S_2 to be conducting and diodes D_1, D_2, D_3 and D_4 are cut off, as shown in Figure 2. The currents i_{L1} and i_{L2} through the inductors increase, as does the energy stored in them. The reverse voltages of diodes D_4 and D_2 are forced to be clamped to (V_{C4} - V_{C2}) and (V_{C3} - V_{C1}) respectively, while for diodes D_1 and $D3$, the reverse voltages are forced to be clamped to V_{C1} and $VC2$, respectively.

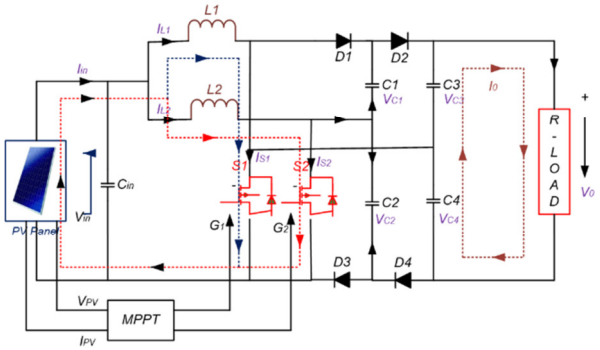


Fig. 2. Equivalent circuit connections for operational mode I.

The load is powered by capacitors C_3 and C_4. The equations showing the voltage between the capacitors are listed below:

$$V_{in} = L_1 * \frac{di_{L1}}{dt} = L_2 * \frac{di_{L2}}{dt} \quad (1)$$

$$C_1 * \frac{dV_{c1}}{dt} = C_2 * \frac{dV_{c1}}{dt} = 0 \quad (2)$$

$$C_3 * \frac{dV_{C3}}{dt} = C_4 * \frac{dV_{C4}}{dt} = -(\frac{V_{C3}+V_{C4}}{R}) \quad (3)$$

2) Mode II: ($t_1 \leq t < t_2$)

The corresponding circuit connections and flow of current for mode II are shown in Figure 3. During this mode, S_2 is turned off for the duration of the pause. D_2 and D_3 are still conducting, as is switch S_1. Figure 3 depicts the current flow. C_1 discharges into C_3 of the output capacitor through inductor L_2. Energy from the inductor L_2 is stored in C_2. In this mode, the inductor current i_{L2} falls linearly and the capacitance-voltage V_{C3}=V_{C2}+V_{C1} rises constantly.

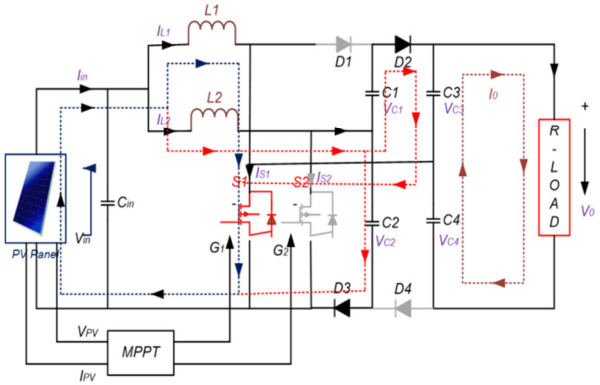


Fig. 3. Equivalent circuit connections for Operational Mode II.

The voltage components in this mode are:

$$V_{in} = L_1 * \frac{di_{L1}}{dt} \quad (4)$$

$$V_{in} - V_{c2} = L_2 * \frac{di_{L2}}{dt} \quad (5)$$

$$C_1 * \frac{dV_{c1}}{dt} = I_{C2} - I_{L2} \quad (6)$$

$$C_2 * \frac{dV_{C2}}{dt} = I_{C1} + I_{L2} \quad (7)$$

$$C_3 * \frac{dV_{C3}}{dt} = -I_{C1} - (\frac{V_{C3}+V_{C4}}{R}) \quad (8)$$

$$C_4 * \frac{dV_{C4}}{dt} = -(\frac{V_{C3}+V_{C4}}{R}) \quad (9)$$

3) Mode III: ($t_2 \leq t < t_3$)

This mode has a similar operation as mode I with the currents in the inductors shown in Figure 4. Therefore, the dynamics in this mode are similar to those in mode I.

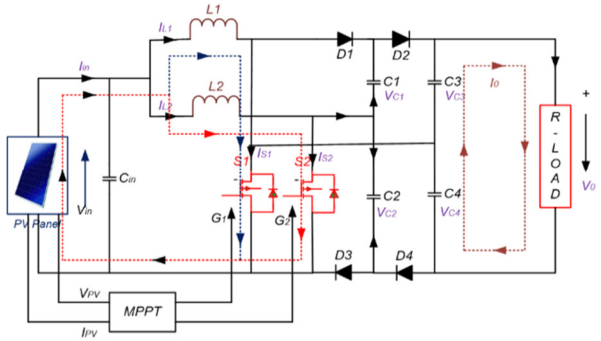


Fig. 4. Equivalent circuit connections for Operational Mode III.

4) Mode IV: ($t_3 \leq t < t_4$)

The equivalent circuit connections along with the current flow directions for mode IV operation are shown in Figure 5. S_2 is turned on, and S_1 is turned off during this mode of operation. D_1 and D_4 were also retained in an ON state. The inductor L_1 and the capacitor C_2 store energy, which is eventually discharged when the load and the output capacitor C_4 are closer together. V_{C4}=V_{C2}+V_{C1} is the voltage across the output capacitor. While the inductor current i_{L2} continuously increases, i_{L1} drops linearly.

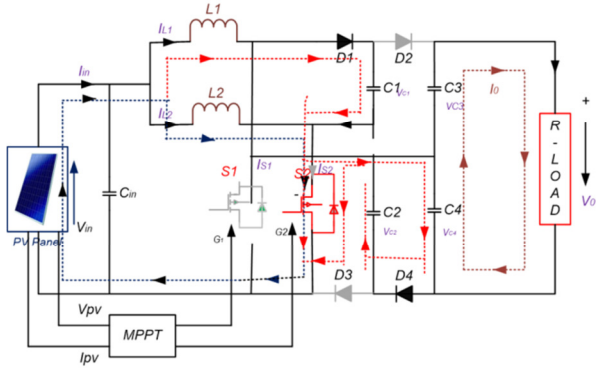


Fig. 5. Equivalent circuit for Operational Mode-IV.

$$L_1 * \frac{di_{L1}}{dt} = V_{in} - V_{C4} + V_{C2} = V_{in} - V_{C1} \quad (10)$$

$$V_{in} = L_2 * \frac{di_{L2}}{dt} \quad (11)$$

$$C_1 * \frac{dV_{C1}}{dt} = i_{C2} + i_{L1} \quad (12)$$

$$C_2 * \frac{dV_{C2}}{dt} = i_{C1} - i_{L1} \quad (13)$$

$$C_3 * \frac{dV_{C3}}{dt} = -(\frac{V_{C3}+V_{C4}}{R}) \quad (14)$$

$$C_4 * \frac{dV_{C4}}{dt} = -i_{C2} - (\frac{V_{C3}+V_{C4}}{R}) \quad (15)$$

The suggested converter's symmetrical mode of operation makes implementation simple. Furthermore, the functional waveforms in Figure 6 depict minimal voltage stress and uniform current distribution in active switches and diodes.

III. MATHEMATICAL ANALYSIS OF PERFOMANCE INDICES

The capacitor voltage ripple is taken to be zero for the purposes of a more straightforward analysis. The following provides a direct calculation of the voltage stresses of the power switches. Volt-sec balance for inductors is given in (16) and (17). Applying the charge-sec balance for capacitors results in the expressions provided in (17). The KVL in the output loop results in the output voltage as given in (18) and the equivalent duty ration is provided in (19). The voltage stress across the switch is the voltage under the OFF condition of the switch. Thus, the voltage stress for power switches is given in (20). From (19) and (20), it is observed that the power switch voltage stress accounts for 0.25 pu of the output voltage, as obtained in (21). Hence, the converter under consideration demonstrates the capability to facilitate power conversion for devices with low-voltage ratings. As a result, the reduction in conduction and switching losses is substantial.

$$D * V_{in} + (1 - D) * (V_{in} - V_{C1}) = 0 \quad (16a)$$

$$D * V_{in} + (1 - D) * (V_{in} - V_{C2}) = 0 \quad (16b)$$

The capacitor voltages V_{C3} and V_{C4} are:

$$V_{C3} = V_{C1} + V_{C2} = \frac{2}{1-D} * V_{in} \quad (17a)$$

$$V_{C4} = V_{C1} + V_{C2} = \frac{2}{1-D} * V_{in} \quad (17b)$$

The output voltage is:

$$V_0 = V_{C3} + V_{C4} = \frac{4}{1-D} * V_{in} \quad (18)$$

The duty ratio is defined as:

$$M = \frac{V_0}{V_{in}} = \frac{4}{1-D} \quad (19)$$

The voltage strains experienced by switches S_1 and S_2:

$$V_{S1} = V_{S2} = \frac{1}{1-D} * V_{in} \quad (20)$$

Power switches experience voltage stress when:

$$V_{S1} = V_{S2} = \frac{V_0}{4} \quad (21)$$

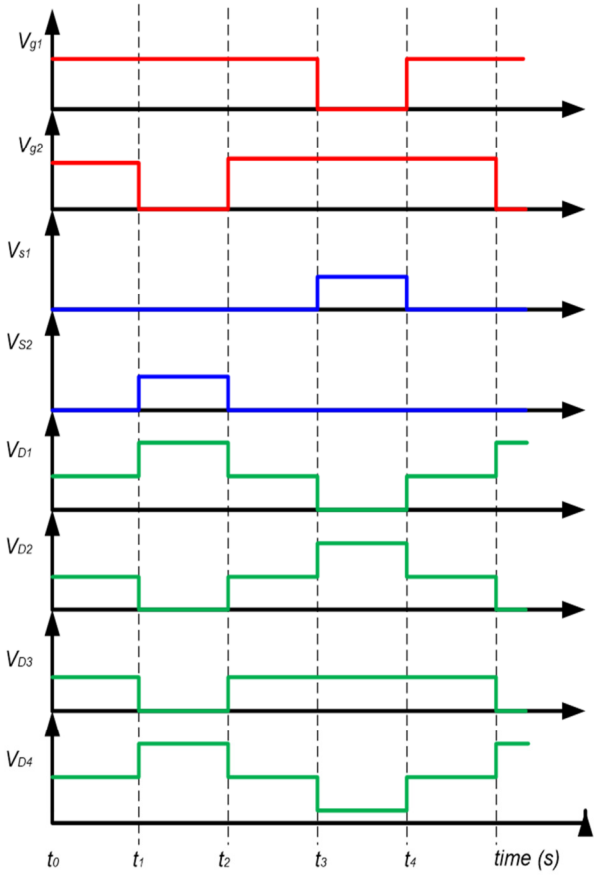


Fig. 6. Switches and diodes one cycle of steady state operation.

IV. SIMULATION AND PERFORMANCE EVALUATION

The converter was tested for interfacing a 25 V, 400 W PV source to a 400 V DC bus using the MATLAB platform. The switching frequency was considered to be 40 kHz to limit the filter component sizing. The duty ratio was set to be 0.75 pertaining to the calculations depicted in Section III. A constant frequency triangular carrier was employed to generate gating signals to the power switches. The simulation parameters are presented in Table I.

TABLE I. SIMULATION PARAMETERS

Parameter	Value
PV panel	25 V, 250 Wp
DC output Voltage	400 V
Load resistance	800 Ω
Duty cycle	0.75
Switching frequency	40 kHz
$L_1 - L_2$	100 µH
$C_1 - C_4$	10 µF
$S_1 - S_2, D_1 - D_4$	400 V, 5 A

The voltage input and output of the proposed circuit are shown in Figure 7. It can be seen that the steady DC voltages at the input and output buses of the converter signify the proposed high gain operation using the interleaved operation together with the voltage multiplier.

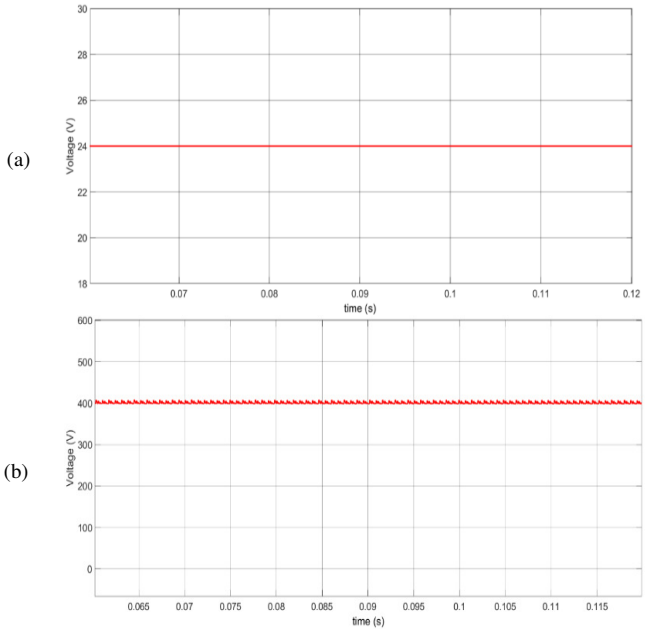


Fig. 7. (a) PV Bus voltage; (b) output voltage.

The intermediate steady voltages across the multiplier cell capacitors and the output regulating capacitors are shown in Figure 8. The steady voltage of 0.25 pu of output voltage is verified across the capacitors C_1 and C_2 as obtained in Section III. Also, the time shift in the ripple voltage of multiplier cell capacitors C_1 and C_2 as seen from Figure 8 accounts for lessened ripple in the output regulating capacitors C_3 and C_4. The steady voltage of 0.5 pu of the output voltage is verified across the capacitors C_3 and $C4$ as obtained in Section III. Also, the time shift in the ripple voltage of multiplier cell capacitors C_3 and $C4$, as seen in Figure 8 accounts for lessened ripple in the output voltage.

The voltage stress across the multiplier cell diodes is studied to verify the power rating. Figure 9 depicts the turn ON duration and reverse voltage across the diodes under steady operation. The reverse voltage is obtained to be 100 V which is 0.25 pu of the output voltage as obtained in Section III. The turn ON duration of D_1 and D_3 is high as it appears in two modes of operation compared to its complementary pair.

V. PERFORMANCE ANALYSIS

Figure 10 compares the voltage gain characteristics of standard interleaved converters with the proposed converter. A minimum of double the gain is achieved with the designed topology compared to the multiphase interleaved converter as proposed in [14] or the voltage multiplier topology proposed in [15] or the high gain conversion interleaved topology with integrated built-in transformer proposed in [16] for any duty cycle in the nominal operational range. For higher duty ratios, the voltage gain of 1.5 times higher voltage gain is observed with the proposed converter.

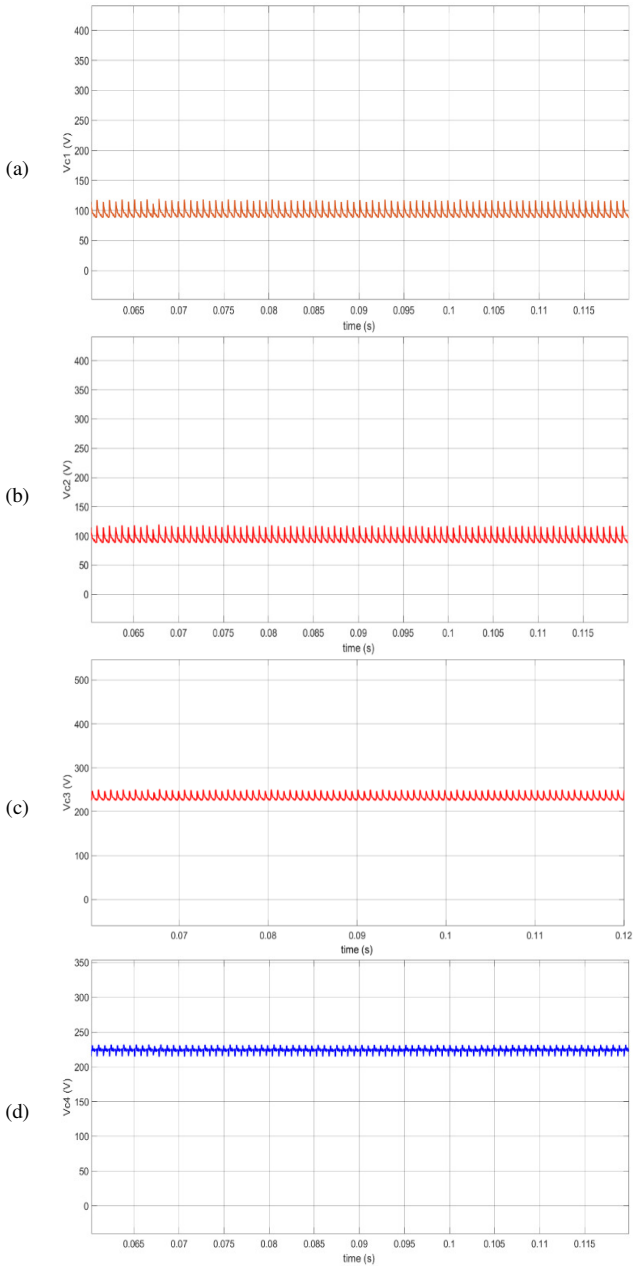


Fig. 8. (a) Capacitor blocking performance V_{c1}, (b) Capacitor blocking performance V_{c2}, (c) output capacitor performance data V_{c3}, (d) output capacitor performance data V_{c4}.

The proposed topology and existing topologies are compared with respect to voltage stress of switching components for various duty cycles. Figure 11 compares the normalized voltage stress characteristics of standard topologies with designed topology. At least 50% reduction in voltage stress is obtained with the proposed converter compared to the multi-phase interleaved converter proposed in [14], by 37.5%

as compared to the voltage multiplier topology proposed in [15], or the high gain conversion interleaved topology with integrated built-in transformer proposed in [16] for any duty cycle in the nominal operational range. For higher duty ratios, the voltage stress on the power switches of the existing converters varies, but the voltage stress on the power switches of the proposed converter remained constant in the nominal operational range to confirm the expression of the voltage stress as obtained in (21).

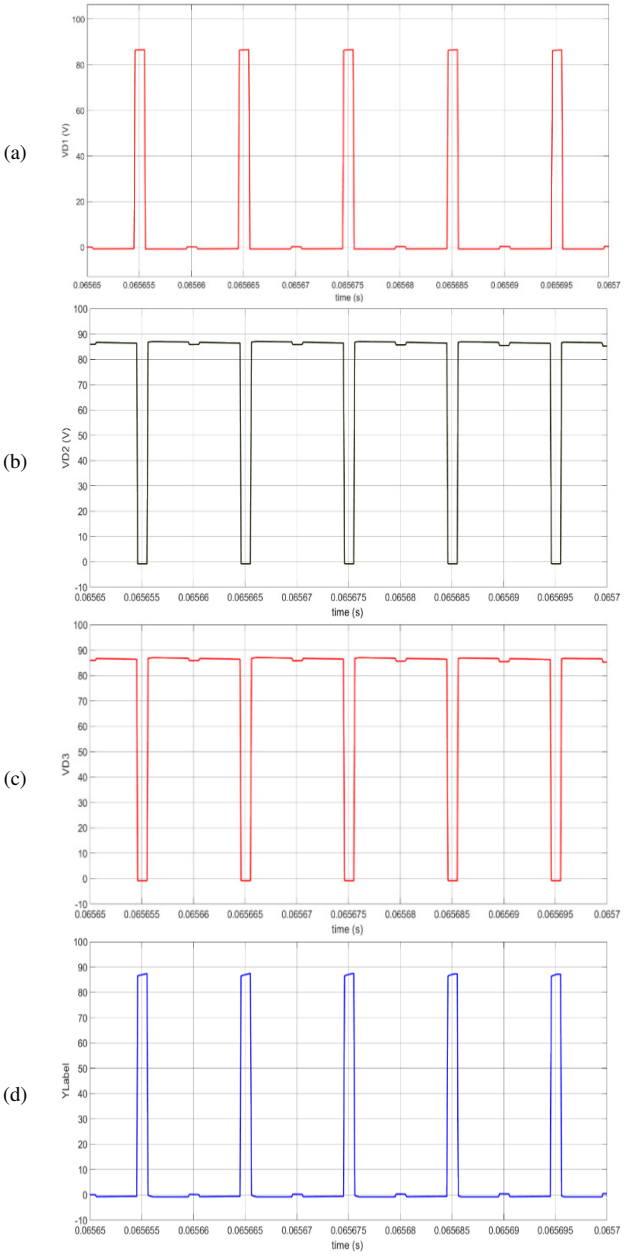
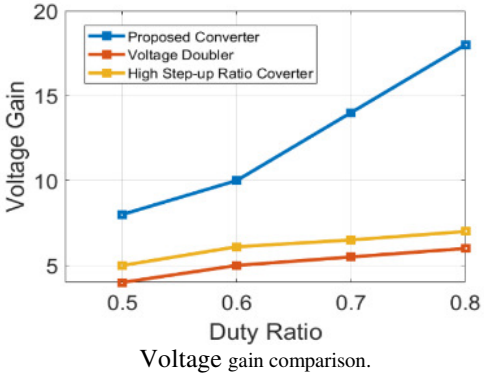


Fig. 9. Voltage stress on diodes (a) V_{D1}, (b) V_{D2}, (c) V_{D3}, and (d) V_{D4}.

Soft switching derived from switching of capacitors and inherent inductor behavior resulted in reduced switching losses, which is equivalent to switch losses with high gain soft switched topologies developed in [22, 25]. The voltage gain and voltage stress for various duty cycle operation are presented in Table II.



Voltage gain comparison.

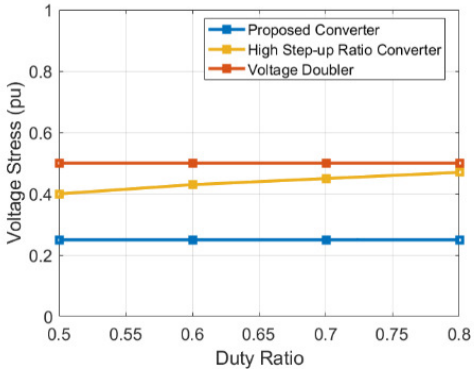


Fig. 10. Voltage stress comparison.

Another advantage of the designed converter is the duty cycle derived from the MPPT algorithm. The algorithm tracking the available maximum PV power provides a duty cycle reference for the next sample. The interleaved switches operate at duty such as to absorb maximum power from PV source. Figure 11 shows the efficiency of the power conversion at various levels of irradiance that correspond to power availability.

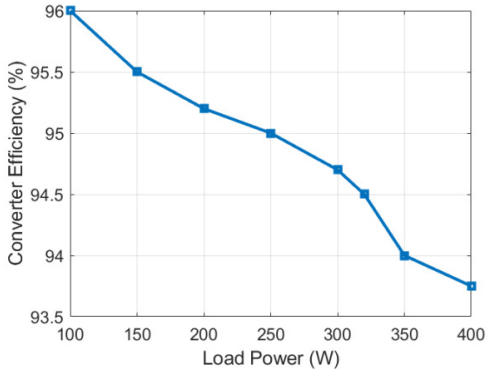


Fig. 11. Efficiency of the converter for varying load power.

TABLE II. COMPARISON OF CONVERTER VOLTAGE GAIN AND POWER SWITCH VOLTAGE STRESS

Converter	Voltage gain vs duty cycle			Voltage stress vs duty cycle			Efficiency vs irradiance		
	0.5	0.6	0.7	0.5	0.6	0.7	0.25 pu	0.5 pu	1 pu
[14]	4	5	6	0.5	0.5	0.5	-	-	-
[15]	4	5	6	0.5	0.5	0.5	95	94	93
[16]	4	5	6	0.5	0.5	0.5	-	-	-
[17]	4	5	6	0.5	0.5	0.5	-	-	-
[21]	5	6.1	7	0.4	0.43	0.45	95.2	94.3	93.2
[24]	5	6.1	7	0.4	0.43	0.45	95	94	93
[25]	5	6.1	7	0.4	0.43	0.45	-	-	-
[26]	-	-	-	0.4	0.4	0.4	94.1	93.4	89.5
[27]	2.9	5.1	9.5	0.4	0.4	0.4	95.3	94.8	91.8
Proposed	8	10	14	0.25	0.25	0.25	96	95.7	93.6

For a power conversion at low irradiance, a maximum efficiency of 96% is observed, while a minimum efficiency of 93.5% is observed at nominal irradiance. Thus, the designed converter generates 2.4 times the energy of the converter proposed in [15]. Also, the converter topologies proposed in [16-18] do not resort to MPPT tracking. Therefore, the proposed converter combines the merits of soft-switched interleaved conversion with maximum power tracking control. Thus, these findings serve to enhance soft switched interleaved boost converter for high voltage gain without need for transformer and therefore aid for minimal component systems with high power and energy efficiency in high voltage gain DC-DC power conversion.

The size of the interleaved inductors for the desired maximum ripple current is obtained as follows.

From (4) and (19), respectively, we get:

$$L_1 = \frac{D}{2f_{sw}\Delta i_{L1}} v_{in} \quad (22)$$

$$D = 1 - \frac{16*V_{in}}{V_0} \quad (23)$$

To obtain the worst-case duty cycle, consider the range of PV voltage varying from 22 V to 26 V in the operating range of irradiance, the duty cycle varies from 0.545 to 0.615. Substituting the maximum value of the operating duty cycle, the size of the inductor L_1 can be determined as:

$$L_1 = \frac{0.615*22}{2f_{sw}\Delta i_{L1}} \quad (24)$$

The size of the multiplier capacitors for the desired maximum ripple-cin output voltage is obtained from (3) and (9) as follows:

$$C_3 = \frac{D}{2f_{sw}\Delta v_0} v_0 \quad (25)$$

$$C_4 = \frac{D}{2f_{sw}\Delta v_0} v_0 \quad (26)$$

Now, according to the multiplier principle,

$$C_1 = C_2 = \frac{D}{4f_{sw}\Delta v_0} v_0 \quad (27)$$

The efficiency obtained at various irradiance levels as depicted in Table II proves the robustness of limiting inductor ripple current and thus aiding in higher efficiency of the converter.

VI. CONCLUSION

A high-gain symmetrical multiplier-based interleaved DC to DC boost converter is developed for photovoltaic (PV) conversion application. A high gain of 16 is achieved in voltage conversion with a low duty cycle range of 0.5 – 0.7 for the nominal irradiance range. Both conduction and switching losses are decreased by the low voltage stress of 0.25 pu. The ability to share current symmetrically without additional circuits is presented by the proposed topology. The efficiency of the converter is better than 93.75% even for the lowest irradiance. The results obtained show that the designed converter performs better in situations where a large voltage gain is needed. The proposed converter serves as a basis for achieving high-efficiency power conversion for DC microgrid applications. This converter has the scope to include bi-directional power conversion with the addition of power switches. Also, soft switching can be achieved in the forward power transfer direction. These aspects can be extended further with the inclusion of real non-idealities for the power switches and the filter elements and using SPICE platforms.

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